AMENDMENTS TO THE CLAIMS

Please amend claims 1-6 as follows:

1. (currently amended) A semiconductor device having a lower pattern density in an edge area than in a central area of a wafer, comprising:

a plurality of parallel but staggered active bar-type patterns ~~allocated at a predetermined distance in~~ formed on the central area of the wafer;

a plurality of parallel but staggered dummy bar-type patterns formed ~~in~~ on the edge area of the wafer; and

a plurality of a connection ~~pattern~~ patterns extending perpendicular to the active bar-type and dummy bar-type patterns; at least one connection pattern adapted to couple at least two of the staggered and adjacent active bar-type patterns to each other and a plurality of other connection patterns each adapted to couple two of the staggered and adjacent dummy bar-type patterns to each other;

wherein the connection patterns coupling two of the plurality of dummy patterns together are parallel to each other but staggered with respect to each other ~~is allocated in a zigzag fashion~~.

2. (currently amended) The semiconductor device as recited in claim 1, wherein the active bar-type ~~pattern is a pattern~~ patterns are for a device isolation layer or a landing plug contact.

3. (currently amended) The semiconductor device as recited in claim 2, wherein the dummy pattern includes:

a first dummy bar-type pattern;

a second dummy bar-type pattern allocated at a predetermined distance from the first dummy bar-type pattern; and

the connection pattern is adapted to connect the first bar-type pattern to the second bar-type pattern.

4. (currently amended) The semiconductor device as recited in claim 3, wherein the first and the second dummy bar-type patterns are in a range of about 80% to about 120% of the size of the active bar-type ~~pattern~~ patterns in the central area of the wafer.

5. (currently amended) The semiconductor device as recited in claim 1, wherein the dummy ~~pattern include~~ bar-type patterns include N number of dummy bar-type patterns ~~allocated at~~ disposed a predetermined distance between ~~two bar-type patterns~~ themselves, where N is a positive integer, and wherein at least two dummy bar-type patterns of the N number of dummy bar-type patterns are connected.

6. (currently amended) The semiconductor device as recited in claim 5, wherein ~~the~~ a size of the dummy bar-type patterns ~~is in~~ ranges from about 80% to about 120% of the size of the active bar-type ~~pattern~~ patterns in the central area of the wafer.

7. (original) The semiconductor device as recited in claim 1, wherein the central area and the edge area are a cell center area and a cell edge area, respectively.

8. (original) The semiconductor device as recited in claim 1, wherein the central area is a core cell area and the edge area is a peripheral area.